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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/902,691	07/12/2001	Li Li	M4065.0159/P159-A	3130

24998 7590 07/08/2004

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/902,691	LI ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on th cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *59,60,62,64,66-84,92 and 93* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *59,60,62,64,66-84,92 and 93* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on November 1, 2002. These drawings are approved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 92 – 93 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for "said cured photoresist layer comprising a plurality of openings formed in said cured photoresist layer, said plurality of openings having reduced striations resulting from the application of a first power level plasma of an etching gas to the integrated circuit substrate for a first predetermined time" can be found.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 59 – 60, 68 – 84, 92 – 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mukai (USPAT 4920070) in view of Manocha (USPAT 4554048).

With regard to claim 59, Mukai discloses in figures 8a – 8h an integrated circuit substrate. Mukai discloses in figure 8b and column 8, line 41 an oxide layer (503) formed over the substrate. Mukai discloses in figures 8c – 8d and column 8, lines 55 – 59 a plurality of cylindrical contact holes (3) formed in the oxide layer, the plurality of contact holes having sidewalls which have a substantially uniform profile and are formed of the same material as the material of the oxide layer, the plurality of contact holes extending to a topmost surface of the oxide layer (21). It is not clear if Mukai teaches that the contact holes have reduced sidewall striations, thereby reducing critical dimension loss between the contact holes. Manocha teaches in figures 1a – 1b, figure 2, and column 3, lines 13 – 39 applying a first power level plasma of an etching gas to an integrated circuit substrate (10) for a first predetermined time followed by the application of a second power level plasma of the etching gas to the integrated circuit substrate for a second predetermined time, wherein the second power level plasma is higher power plasma than the first power level plasma. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the plasma treatment of Manocha in the device of

Mukai in order to reliably produce vertical sidewalls and thus improve device yields as stated by Manocha in column 1, line 6 – column 2, line 10. It would have been further obvious in the device of Mukai and Manocha that the cylindrical contact holes produced would result in having reduced sidewall striations, thereby reducing critical dimension loss between the contact holes. It is noted that the limitations in claim 59 following, and including, "said reduced striations resulting from the application of a first power level plasma..." are product-by-process limitations that do not patentably distinguish the claimed invention over the prior art.

With regard to claim 60, Mukai discloses in figures 8a – 8h and column8, line 43 wherein the substrate (1) is a silicon-based substrate.

With regard to claim 92, Mukai discloses in figures 8a – 8h an integrated circuit substrate (1). Mukai discloses in figure 8b and column 8, line 41 an oxide layer (21) formed over the substrate. Mukai discloses in figures 8b – 8d and column 8, lines 55 – 59 a photoresist layer (inherent in the photolithography process) formed over and in contact with the oxide layer, the photoresist layer comprising a plurality of openings formed in the photoresist layer. As far as the examiner can ascertain, Mukai discloses in figures 8b – 8d and column 8, lines 55 – 59 the plurality of openings have reduced striations. Mukai is silent to teaching that the photoresist layer is cured. As far as the examiner can ascertain Manocha teaches in figures 1a – 1b, figure 2, and column 3, lines 13 – 39 a cured photoresist layer (12) formed over and in contact with an oxide layer (11), the photoresist layer comprising at least one opening formed in the photoresist layer, the at least one opening having reduced striations resulting from the application of a first power level plasma of an etching gas to the integrated circuit substrate for a first predetermined time. It would have been obvious to one of ordinary skill in the art at the time of the present

invention to use the plasma treatment of Manocha in the device of Mukai in order to reliably produce vertical sidewalls and thus improve device yields as stated by Manocha in column 1, line 6 – column 2, line 10. Mukai discloses in figures 8b – 8d and column 8, line 41 a plurality of recesses (3) formed in the oxide layer and adjacent the plurality of openings in the photoresist layer, sidewalls of the recesses forming sidewalls of cylindrical contact holes extending to a topmost surface of the oxide layer. It would have been further obvious in the method of Mukai and Manocha that the photoresist layer is cured. Mukai is further silent to reduced striations in the plurality of recesses in the oxide layer. Manocha teaches in figures 1a – 1b, figure 2, and column 3, lines 13 – 39 an application of a second power level plasma of the etching gas to the cured photoresist layer and to the oxide layer for a second predetermined time, wherein the second power level plasma is a higher power plasma than the first power level plasma, and wherein the substrate has a decreased critical dimension loss compared to the critical dimension loss of a substrate formed without the application of the second, higher power level plasma. It would have been further obvious to use the second power level plasma of Manocha to etch the device of Mukai in order to reliably produce vertical sidewalls and thus improve device yields as stated by Manocha in column 1, line 6 – column 2, line 10. It would have been further obvious in the device of Mukai and Manocha that the cylindrical contact holes produced would result in having reduced sidewall striations, thereby reducing critical dimension loss between the contact holes. It is noted that the limitations in claim 92 referring to power level plasmas are product-by-process limitations that do not patentably distinguish the claimed invention over the prior art.

With regard to claims 68 – 84, and 93 – 95 Mukai and Manocha read on claimed limitations. It is noted that the limitations in claims 68 – 84, and 93 are product-by-process claims that do not patentably distinguish the claimed device over the prior art.

6. Claims 62, 64 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mukai and Manocha as applied to claim 59 above, and further in view of Summerfelt et al. (USPAT 5612574, Summerfelt).

It is not clear if Mukai and Manocha teach the substrate is a gallium arsenide substrate, a germanium substrate, or a DRAM substrate. Summerfelt discloses in figure 1 and column 3, lines 3 – 11 wherein the substrate is a germanium substrate. Summerfelt discloses in figure 1 and column 3, lines 3 – 11 wherein the substrate is a gallium arsenide substrate. Summerfelt discloses in figure 1 and column 2, lines 3 – 8 wherein the substrate is a DRAM substrate. It would have been obvious to use the substrates of Summerfelt in the device of Mukai and Manocha in order to use the most efficient and appropriate substrate for the intended application of the device.

7. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mukai and Manocha as applied to claim 59 above, and further in view of Foote et al. (USPAT 5710067, Foote).

It is not clear if Mukai and Manocha disclose an antireflective coating. Foote discloses in column 1, lines 21 – 48 wherein a substrate has an antireflective coating thereon. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the

antireflective coating of Foote in the method of Mukai and Manocha in order to exhibit the requisite optical parameters to suppress multiple interference effects caused by the interference of light rays propagating in the same direction due to multiple reflections in the photoresist film as stated by Foote in column 1, lines 21 – 48.

Response to Arguments

8. Applicant's arguments with respect to claims 59, 60, 62, 64, 66 – 84, 92, and 93 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II